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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re application of:

Hidenori OGATA et al.

Serial No: 09/291,538

Filed:

April 14, 1999

For:

LASER ANNEAL METHOD OF A

SEMICONDUCTOR LAYER

AMENDMENT

Box Non-Fee Amendment Commissioner for Patents Washington, D.C. 20231

Dear Sir:

Art Unit: 2822

Examiner: M.A. Wilczewsk

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Commissioner for Patents Washington D.C. 20231, on

December 20, 2002 Date of Deposit

John P. Scherlacher, Reg. No. 23,009

Name Signature

12/20/02 Date

In response to the Office Action dated June 25, 2002, the period for response to which is being extended to December 25, 2002 by the accompanying Petition, please amend the above-identified application as follows

IN THE CLAIMS:

Rewrite claim 9 as follows:

9. (Amended) A transistor device in which a polycrystal semiconductor layer is formed by subjecting an amorphous semiconductor layer formed on a substrate to laser anneal processing, wherein

an energy level in a region to be irradiated by a laser beam of the amorphous semiconductor layer is set such that the level in a rear area of a region along a scan direction of the laser beam is lower than the upper limit energy level which maximizes a grain size of the semiconductor layer, and